Amendments to the Specification

In the Abstract

Please replace the original Abstract beginning at paragraph 136 with the following rewritten Abstract:

The System-on-Chip apparatus and integration methodology disclosed includes a single semiconductor integrated circuit having one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller (MAC) on a first internal unidirectional bus. The first internal unidirectional bus controls transactions between the processor subsystem(s) ~~the MAC,~~ and the DMA peripheral(s) using a Memory Access Controller (MAC) ~~single centralized address decoder~~ and unidirectional, positive-edge clocked address and transaction control signals. The first internal unidirectional bus can support burst operation, variable-speed pipelined memory transactions, and hidden arbitration. The SoC may include a second internal unidirectional bus that controls transactions between the processor subsystem(s) and non-DMA peripherals. The second internal unidirectional bus controls transactions between the processor subsystem(s) and the non-DMA peripheral(s) using unidirectional address and transaction control signals. Peripherals may be synchronous or asynchronous to their respective buses.

In The Specification

Please amend the specification by replacing paragraph number 14 with the following rewritten paragraph:

It is therefore an object of the present invention to provide a system-on-chip interconnection structure and method for efficient integration of a variety of functional circuits. It is a further object of the present invention to provide an on-chip interconnect architecture that standardizes how systems-on-chip are fabricated on silicon semiconductor integrated circuit chips. The present invention is a System-on-Chip apparatus and integration methodology wherein a single semiconductor integrated circuit includes one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller on a first internal unidirectional bus. The first internal unidirectional bus controls transactions between the processor subsystem(s) ~~the Memory Access Controller~~ and the DMA peripheral(s) using a ~~single centralized address decoder~~ Memory Access Controller and unidirectional address and transaction control signals that are launched and captured on the rising edges of the bus clock signal. The first internal unidirectional bus supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred. In some embodiments, the first internal unidirectional bus includes a bus arbiter that grants access to the first internal unidirectional bus and arbitrates memory accesses for transactions on the first internal unidirectional bus. In some embodiments that include a bus arbiter, arbitrations are "hidden," meaning that the memory access arbitration for a selected transaction may overlap a data transfer

associated with a prior transaction, or may occur in the same clock cycle in which access is granted and data transfer begins for the selected transaction.

Please amend the specification by replacing paragraph number 131 with the following rewritten paragraph:

In sum, the present invention is a System-on-Chip apparatus and integration methodology wherein a single semiconductor integrated circuit includes one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller on a first internal unidirectional bus. The first internal unidirectional bus controls transactions between the processor subsystem(s) ~~the Memory Access Controller~~ and the DMA peripheral(s) using a ~~single centralized address decoder~~Memory Access Controller and unidirectional address and transaction control signals that are launched and captured on the rising edges of the bus clock signal. The first internal unidirectional bus supports pipelined memory transactions, wherein a memory access may occur before data associated with a prior memory access has been transferred. In some embodiments, the first internal unidirectional bus includes a bus arbiter that grants access to the first internal unidirectional bus and arbitrates memory accesses for transactions on the first internal unidirectional bus. In some embodiments that include a bus arbiter, arbitrations are "hidden," meaning that the memory access arbitration for a selected transaction may overlap a data transfer associated with a prior transaction, or may occur in the same clock cycle in which access is granted and data transfer begins for the selected transaction.